AMENDMENTS TO THE ABSTRACT:

Please amend the Abstract as follows:

Please cancel without prejudice the existing Abstract and substitute the following Abstract:

An integrated circuit having a plurality of processing stages includes a low power mode controller operable to control the integrated circuit to switch between an operational mode and a standby mode. At least one of the processing stages has a non-delayed latch to capture a non-delayed value of an output signal from that processing stage and a delayed latch operable during the operational mode to capture a delayed value of the same signal. A difference between these two captured signals is indicative of the processing operation not being completed at the time the non-delayed signal was captured. The delayed latch is operable during the standby mode to retain the signal it captured whilst the non-delayed latch is powered down and loses its value. The delayed latch is formed to have a lower power consumption than the non-delayed latch.